encoding the first parallel data to generate third parallel data of M bits ($M \neq N$);

converting the third parallel data to fourth parallel data of N bits; and

selectively adding an error correction check code to the second parallel data and the fourth parallel data,

said adding step performing a common addition processing irrespectively of the second parallel data and the fourth parallel data. --.

C1 Cont'd.

REMARKS

Claims 22-30 have been cancelled and claims 31-37 have been added. Attached hereto is a marked-up version of the changes made to the claims by this Amendment. This marked-up version has been entitled "Version With Markings To Show Changes Made."

The Examiner has rejected applicants' claims 22-30 under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one of skill in the art to make and use the invention. In particular, the Examiner states that the specification does not describe a converting means for converting the first digital information from N bits to M bits, M being the coding of the second digital signal. The Examiner further argues that the specification does not describe a coding means for outputting M bit data by coding the second digital information.

As above-indicated, claims 22-30 have been deleted. Moreover, newly added claims 31-37 recite inputting first and second parallel data each of N bits, encoding the first parallel data to generate third parallel data of M bits ($M \neq N$), and converting the third parallel data to fourth

parallel data of N bits. These recitations are believed to be supported by the disclosed embodiments in applicants' specification. Accordingly, the Examiner's rejection in this regard has been obviated.

The Examiner has also rejected applicants' claims 22-30 under 35 USC § 103(a) as anticipated by the Sochor patent taken in view of the Yoshimura, et al. patent. Applicants' claims 22-30 have been cancelled, thereby obviating this rejection. Moreover, to the extent the Examiner believes that the Examiner's rejection is applicable to newly added 31-37, the rejection is respectfully traversed.

Applicants' newly added independent claims 31 and 37 are directed to a digital information coding apparatus and method in which an input unit selectively inputs first and second parallel data of N bits representing first and second digital information. An encoder encodes the first parallel data to generate third parallel data of M bits, where $M \neq N$. A converter converts the third parallel data into fourth parallel data of N bits. An error correction unit selectively adds an error correction check code to the second parallel data and the fourth parallel data. The latter unit performs common addition processing irrespectively of the second parallel data and the fourth parallel data.

Such a construction is not taught or suggested by the cited art of record. More particularly, in the Sochor patent a chrominance signal Y and two color difference signals U,V are input as parallel 8-bit signals at an input 21. The parallel signals are reshuffled in buffer 22 and then converted in a buffer 23 from 8-bit signals to 10-bit signals, "this conversion providing at the same time error protection by insertion of parity bits" (see, column 3, lines 55-57, of the

Sochor patent). The signals are then distributed between two channels in the manner shown in FIG. 1 of the patent.

Thus, the Sochor patent is not believed to teach or suggest encoding of one of two N bit signals into an M bit signal, converting of the M bit signal to an N-bit signal and providing error correction to the other of the N-bit signal and to the converted N-bit signal, the error correction performing a common addition irrespectively of the signal. While, the Sochor patent provides error protection, it is to the parallel 10 bit signals which have been converted from the parallel 8-bit signals. There is no encoding of one of the 8-bit signals to a 10-bit signal and conversion of this 10-bit signal back to an 8-bit signal.

The Sochor patent thus fails to teach or suggest applicants' invention of claims 31-37. Moreover, the Yoshimura, et al. patent fails to add anything to the Sochor patent to change this conclusion. Applicants' claims 31-37 thus patentably distinguish over the combination of the Sochor and Yoshimura, et al. patents.

In view of the above, it is submitted that applicants' claims, as amended, patentably distinguish over the cited art of record. Accordingly, reconsideration of the claims is respectfully requested.

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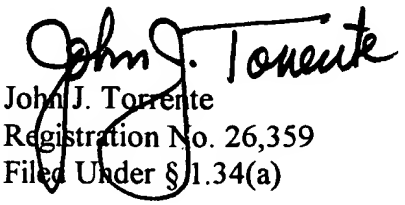
Respectfully submitted,



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Version With Markings To Show Changes Made

Cancel claims 22-30 and add claims 31-37 as follows:

-- 31. A digital information coding apparatus, comprising:

a) an input unit, arranged to selectively inputting a first parallel data of N bits representing a first digital information and second parallel data of N bits representing a second digital information;

b) an encoder, arranged to encode the first parallel data to generate third parallel data of M bits ($M \neq N$);

c) a converter, arranged to convert the third parallel data into fourth parallel data of N bits;

d) an error correction unit, arranged to selectively add an error correction check code to the second parallel data and the fourth parallel data,

said error correction unit performing a common addition processing irrespectively of second parallel data and the fourth parallel data. –

-- 32. An apparatus according to claim 31, wherein said encoder encodes the first parallel data to be encoded by differential pulse code modulation.--.

-- 33. An apparatus according to claim 31, wherein the second digital information is a television signal in which a video signal and an audio signal are time-division multiplexed. --.

-- 34. An apparatus according to claim 31, wherein said error correction unit adds a predetermined data amount of error correction check code for every predetermined data amount of the second parallel data or the fourth parallel data. --.

-- 35. An apparatus according to claim 31, further comprising a recording unit, arranged to record the data processed by said error correction unit on a recording medium. --.

-- 36. An apparatus according to claim 31, wherein the second digital information has a lower bit rate than the first digital information. --.

-- 37. A digital information coding method, comprising:

selectively inputting first parallel data of N bits representing a first digital information and second parallel data N bits representing a second digital information;

encoding the first parallel data to generate third parallel data of M bits ($M \neq N$);

converting the third parallel data to fourth parallel data of N bits; and

selectively adding an error correction check code to the second parallel data and the fourth parallel data,

said adding step performing a common addition processing irrespectively of the second parallel data and the fourth parallel data. --.